REMARKS/ARGUMENTS

After the foregoing Amendment, Claims 1 and 3-28 are currently pending in this application. Claim 2 has been canceled without prejudice. Claims 1 and 3-25 has been amended, and claims 26-28 have been added, to more particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. The Applicants submit that no new matter has been introduced into the application by the Amendment.

Inventorship

The Examiner's presumption that the subject matter of the various claims of the present invention was commonly owned is correct. The joint inventors of the present invention commonly own the subject matter of the various claims of the present invention.

Claim Rejections - 35 USC §102 and §103

The Examiner has rejected Claims 1 and 9-16 under 35 U.S.C. §102(b) and 35 U.S.C. §102(e) as being anticipated by Divan (US Patent No. 5,099,410) and Pearson (US Patent No. 6,717,392), respectively. The Examiner also has rejected Claims 2-8 and 17-25 under 35 U.S.C. §103(a) as being unpatentable over Pearson in combination with Divan.

The present invention is an inverter for converting a DC input voltage into an AC output voltage. The inverter includes a sigma-delta modulation (SDM) controller having an integrator, a sample-and-hold circuit, and a quantizer circuit. The SDM controller produces a modulated output voltage signal according to a reference voltage signal. The integrator produces an integrator output signal

having an integrated output slope according to a difference between a reference voltage signal and a modulated output voltage signal. The inverter may further include a driving circuit and a power inversion stage circuit. The sample-and-hold circuit is electrically connected to the integrator. The quantizer circuit is electrically connected to the sample-and-hold circuit and to an input terminal of the integrator circuit through an output terminal thereof. The driving circuit is electrically connected to the SDM controller. The power inversion stage circuit is electrically connected to the driving circuit.

Regarding the rejections of claims 1 and 17, Divan discloses a single phase AC power conversion apparatus. Pearson discloses a signal generator. The Applicants submit that neither Divan nor Pearson, alone or in combination, teach or suggest the features of amended claims 1 and 17. Specifically, the Examiner asserts that Pearson discloses an SDM controller that includes an integrator circuit and a quantizer circuit, but fails to point out where these elements are disclosed with reference to claim 2. Based on the Examiner's comments with respect to claim 17, Pearson discloses a controller shown in Figures 2 or 3 that includes an integration circuit 20/22/23 and a quantizer circuit (the Applicants assume the Examiner is referring to reference numeral 21, but the Examiner fails to specify this). As disclosed by Pearson, Figure 2 illustrates a first-order modulator and Figure 3 illustrates a second order modulator.

The Applicants respectfully submit that each of the modulators in Figures 2 and 3 of Pearson perform addition, subtraction and delay functions, <u>not an integration function</u>. The Examiner is respectfully requested to review the integration circuit 111 of Figure 2 in the Applicants' disclosure in conjunction with the written description in paragraphs [0063] - [0069] of pages 12-15. By definition, an integrator outputs a voltage whose rate-of-change (i.e., slope) over change is

proportional to the input's magnitude. Amended claims 1 and 17 recite that the integrator produces an integrator output signal having an integrated output slope according to a difference between the reference voltage signal and the modulated output voltage signal. Neither Pearson nor Divan teach or suggest this feature. Other differences between the present invention and the Pearson and Divan references are described below.

Firstly, Pearson discloses an accumulation stage (20) and a quantization stage (21) electrically connected to the accumulation stage (20) as shown in Fig. 2, and a first accumulator (30), a second accumulator (20) electrically connected to the first accumulator (30), and a quantizer (21) electrically connected to the second accumulator (20) as shown in Fig. 3, and does not disclose the sample-and-hold circuit electrically connected to the integrator circuit for sampling and holding the integrator output signal.

Secondly, the Divan discloses an integrator circuit (106), a bang-bang limiter (107) electrically connected to the integrator circuit (106), and a sample and hold circuit (108) electrically connected to the bang-bang limiter (107) as shown in Fig. 8 and does not disclose a quantizer circuit. In Pearson, the accumulation device (20)/the first accumulator (30)/the second accumulator (20) each has a similar function as an integrator circuit. In Divan, the bang-bang limiter (107) has a similar function as a quantizer circuit. Thus, the proposed inverter including an SDM controller having an integrator, a sample-and-hold circuit, and a quantizer circuit is not suggested or taught by Pearson or Divan.

Furthermore, in Pearson, the teaching relevant to the present invention is that the quantization stage (21) (corresponding to a quantizer circuit) is electrically connected to the accumulation stage (20) (corresponding to an integrator circuit) to form the first-order Δ-Σ modulator as shown in Fig. 2. In Divan, the teaching

relevant to the present invention is that the bang-bang limiter (similar to a quantizer circuit) is coupled between the integrator (106) and the sample and hold circuit (108) to form the sigma delta modulator as shown in Fig. 8. Thus, one with an ordinary skill in the field would be taught by Pearson in combination with Divan at the time of the invention that an SDM controller would have the configuration of an integrator, a quantizer circuit (or a bang-bang limiter) electrically connected to the integrator, and a sample-and-hold circuit electrically connected to the quantizer circuit (or a bang-bang limiter). The above-mentioned deduced configuration of the SDM controller taught by the Pearson in combination with Divan is different from that of the present invention since the sample-and-hold circuit (112) is electrically connected to the integrator (111) and the quantizer circuit (113) is electrically connected to the sample-and-hold circuit (112) as shown in Fig. 2 of the present invention instead of the quantizer circuit (113) is electrically connected to the integrator (111) and the quantizer circuit (113) is electrically connected to the sample-and-hold circuit (112) according to the deduced configuration taught by Pearson in combination with Divan.

The operational principles of the present invention are different from those of the teachings of Pearson in combination with Divan due to the aforementioned different configurations. As pointed out on paragraph [0063], lines 8-15, of the specification and as shown in Fig. 2 of the present invention, the SDM controller (11) is employed to transfer the input reference voltage signal into a modulated output voltage signal (a series of pulse signals/a pulse train) firstly. The frequency of the pulse signals is decided by the frequency of sampling secondly. If the reference voltage signal has a higher voltage level, the output pulses will have a higher density, and if the reference voltage signal has a lower voltage level, the output pulses will have a lower density thirdly. But as described on column 8, lines

61 to 68, and column 9, line 1, and as shown in Fig. 8 of Pearson, the output of the integrator circuit (106) is provided to a bang-bang limiter (107) (having the similar function of a quantizer circuit), and the output of which is provided to a sample and hold circuit (108) firstly. The sample and hold circuit (108) receives a signal at the sampling frequency on a line (109) and provides an output signal on a line (110) during each sampling pulse which is equal to the input to the sample and hold circuit (108) at the time of the sampling pulse on the line (109) secondly. This output is held until the next sampling pulse thirdly. Since in each cycle of the sampling, the output of the integrator circuit (106) is limited by the bang-bang limiter firstly and inputted to the sample and hold circuit (108) secondly as disclosed by the teaching of Pearson in combination with Divan, switching frequency of the switches would be limited by the bang-bang limiter. But in the present invention, the frequency of the pulse signals could be decided by the frequency of sampling as mentioned above, and the switching frequency of the switches could be decided according to the frequency of the pulse signals. Thus, the operational principles of the present invention are totally different from those disclosed by Pearson and Divan.

Since the frequency of the pulse signals could be decided by the frequency of sampling in the present invention, the switching frequency of the switches could be decided according to the frequency of the pulse signals, and the losses of the switches could be lowered by adjusting the switching frequency accordingly. Furthermore, the harmonics generated around the switching frequency of the switches could be detected easily through deciding the frequency of the pulse signals and recognizing the switching frequency of the switches so as to decrease the distortions caused by the harmonics in the present invention. These two advantages of the present invention are not suggested or taught by Pearson or

Divan, alone or in combination. According to the configuration taught by Pearson in combination with Divan, the outputs of the integrator circuit are limited by the bang-bang limiter (or a quantizer circuit) firstly, and thus the frequency of the pulse signals could not be decided by the frequency of sampling secondly, and the switching frequency of the switches could not in turn be adjusted accordingly thirdly.

Accordingly, Applicant requests reconsideration and withdrawal of the rejections directed to Claims 1 and 17. Furthermore, Claims 3-16 and 26 are dependent upon claim 1, and claims 18-25 and 27 are dependent upon claim 17, which the Applicants believe are allowable over the cited prior art of record for the same reasons provided above. Furthermore, new claim 28 is also believed to be allowable over the cited prior art of record for the same reasons provided above.

For the above reasons, the Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. 102 and 35 U.S.C. 103.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1 and 3-28, is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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